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AU6982

USB2.0

Universal Flash Disk Controller Technical Reference Manual

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Contact Information:

Web site: <http://www.alcormicro.com/>

Taiwan

Alcor Micro Corp.
4F, No 200 Kang Chien Rd., Nei Hu,
Taipei, Taiwan, R.O.C.
Phone: 886-2-8751-1984
Fax: 886-2-2659-7723

China ShenZhen Office

Rm.2407-08 ,Industrial Bank Building
No.4013, Shennan Road,
ShenZhen,China. 518026
Phone: (0755) 8366-9039
Fax: (0755) 8366-9101

Santa Clara Office

2901 Tasman Drive, Suite 206
Santa Clara, CA 95054
USA
Phone: (408) 845-9300
Fax: (408) 845-9086

Los Angeles Office

9070 Rancho Park Court
Rancho Cucamonga, CA 91730
USA
Phone: (909) 483-9900
Fax: (909) 944-0464



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1.0 Introduction

1.1 Description

The AU6982 USB 2.0 Flash Disk Controller is the best solutions for SLC (Single-Level Cell), MLC (Multi-Level Cell) NAND and AG-AND with multiple dies data flash. Its high-speed read and write access performance enable users to transfer and backup data effectively. Besides, AU6982 is certified by USB-IF (USB Implementers Forum), WHQL (Window Hardware Quality Labs) and EMI tests to guarantee the quality and reliability for end-users.

With multiple functions integrated into one chip and external components built inside, AU6982 is pledged to deliver the best performance benchmark and to further reduce the BOM cost of end products adopting this solution. It provides dual channel access and ISP (In-System Programming) technologies, which are the most important features to allow manufacturers building high performance UFD easily and to have the flexibility of adopting different source of flash chips. Same as its siblings of product family, AU6982 features the auto-run function to prompt the designated AP automatically when plugging into PC. In addition to being as a removable storage device, AU6982 can also be configured as a bootable disk for system recovery. Also, its random access performance exceed the minimum requirement of Read Boost feature found in Microsoft Vista operating system, in which randomly access blocks of information are saved into UFD for boosting up the average performance.

To enhance the usefulness and manageability of UFD further, Alcor Micro develops a smart application program iStar (Partition/Password Operation Tool) as a handy utility in managing partition, password and security. Having iStar as the companion of UFD, the data in a UFD could be protected from unauthorized access successfully.

1.2 Features

- PCBs are pin-compatible with AU6980, AU6981 and AU6982.
- Integrates built-in regulator
- Supports SLC and MLC dual channel with high performance
- Supports firmware upgrade mechanism (ISP, In-System Programming)
- Integrates hardware DMA engine to tune up the operation performance
- Integrates multi-bit ECC correction mechanism
- Complies with the standards defined in USB v2.0, USB Device Class Definition for Mass Storage and Bulk-Transport v1.0
- Works with default driver under the environments of Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X. Using Alcor Micro's vendor driver for the environment under Windows 98SE
- Concurrent bus operation using multiple FIFO for better performance
- Integrates into flash memory power control switch
- Supports bad block management
- Supports dynamic serial number modification via mass production software
- Supports software write protection



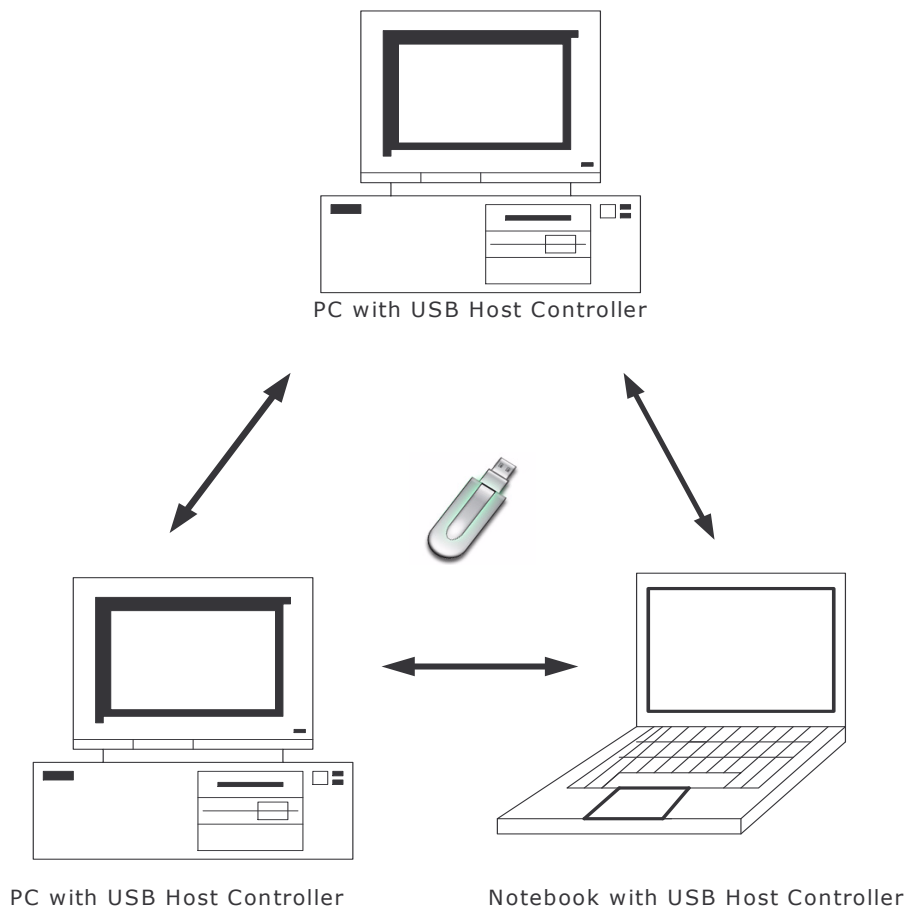
- Supports Auto Run function
- Supports erasable and read-only mode AP Disk
- Supports Ready Boost feature of Microsoft Vista operating system
- Companion application program with UFD – iStar available for users
 - To have UFD partition management function
 - To do password protection for the security in data access
 - To guard data files with software write protection function
 - To lock up PC by UFD as the key
- Available in 48-pin LQFP 7x7mm package to support 4CE pin flash
- Available in 64-pin LQFP 7x7mm package to support 4CE pin flashx4pcs



2.0 Application Block Diagram

The following figure shows the application diagram of a typical flash disk product with AU6982. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6982 is then turned into a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Block Diagram



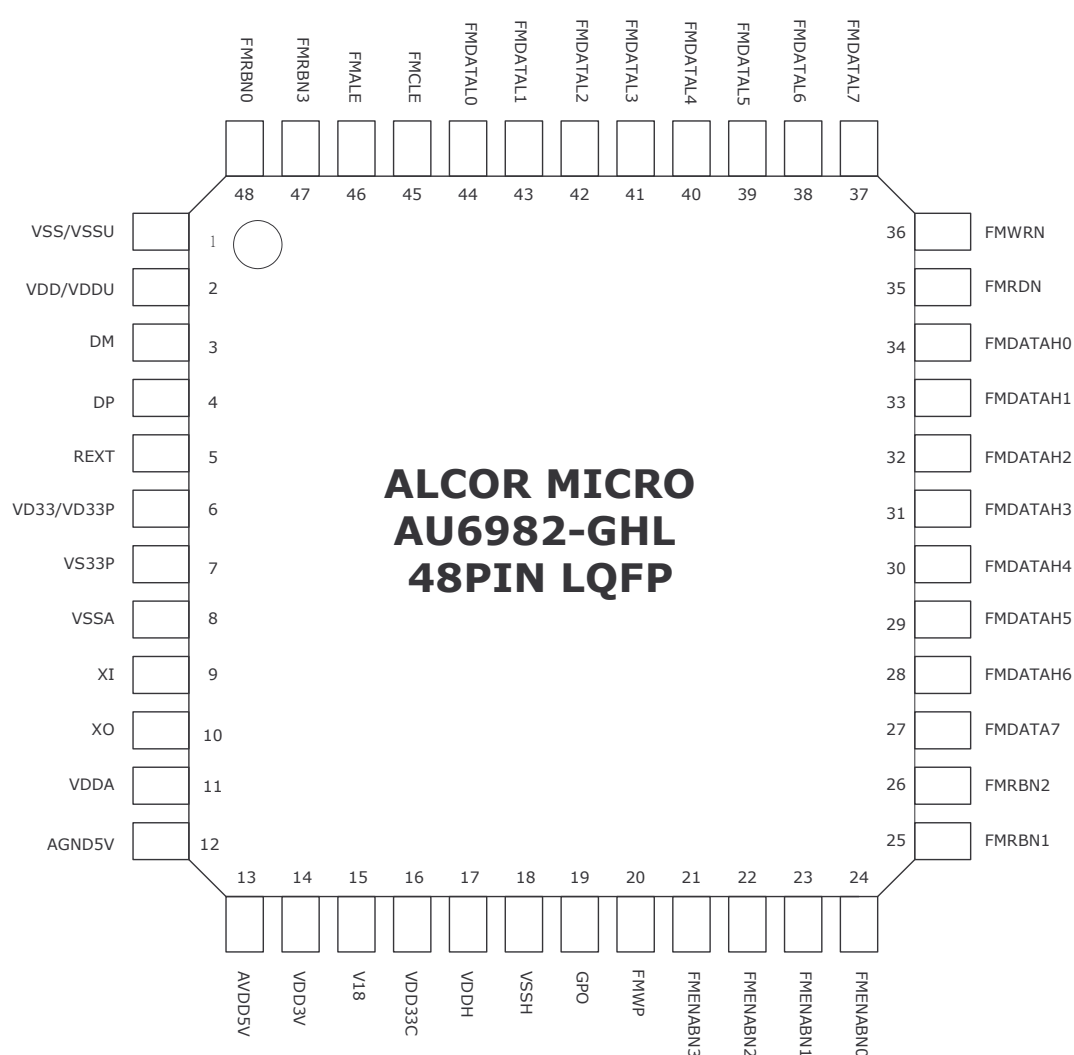


3.0 Pin Assignment

There are two different form factor packages available to choose from. The following figure shows signal names of each pin and the table in the page after describes each pin in details.

3.1 48Pin AU6982-GHL

Figure 3.1 48 Pin Assignment Diagram



**Table 3.1 48 Pin Descriptions**

Pin #	Pin Name	I/O	Description
1	VSS/VSSU	GND	Ground
2	VDD/VDDU	I	1.8V Power Source for Core / 1.8V Power Source for UTMI
3	DM	I/O	USB DM
4	DP	I/O	USB DP
5	REXT	I	External 330 Resister to Ground
6	VD33/VD33P	I	3.3V Power Source for UTMI
7	VS33P	GND	Ground
8	VSSA	GND	Ground
9	XI	I	12 MHz crystal input.
10	XO	O	12 MHz crystal output.
11	VDDA	I	1.8V Power Source for PLL
12	AGND5V	GND	Ground
13	AVDD5V	I	5V Power Source
14	VDD3V	O	3.3 V Power Out
15	V18	O	1.8V Power Out for Core
16	VDD33C	O	3.3V Power Out for Flash Memory
17	VDDH	I	3.3V Power Source for IO pad
18	VSSH	GND	Ground
19	GPO	O	General Purpose OutPut
20	FMWP	I	Flash Memory Write Protect; High Active
21	FMENABN3	I/O	Flash Memory #3 Enable; Low Active
22	FMENABN2	I/O	Flash Memory #2 Enable; Low Active
23	FMENABN1	I/O	Flash Memory #1 Enable; Low Active
24	FMENABN0	I/O	Flash Memory #0 Enable; Low Active
25	FMRBN1	I	Flash Memory(H1) Ready and Busy Signal (1=Ready ; 0=Busy)
26	FMRBN2	I	Flash Memory(H2) Ready and Busy Signal (1=Ready ; 0=Busy)



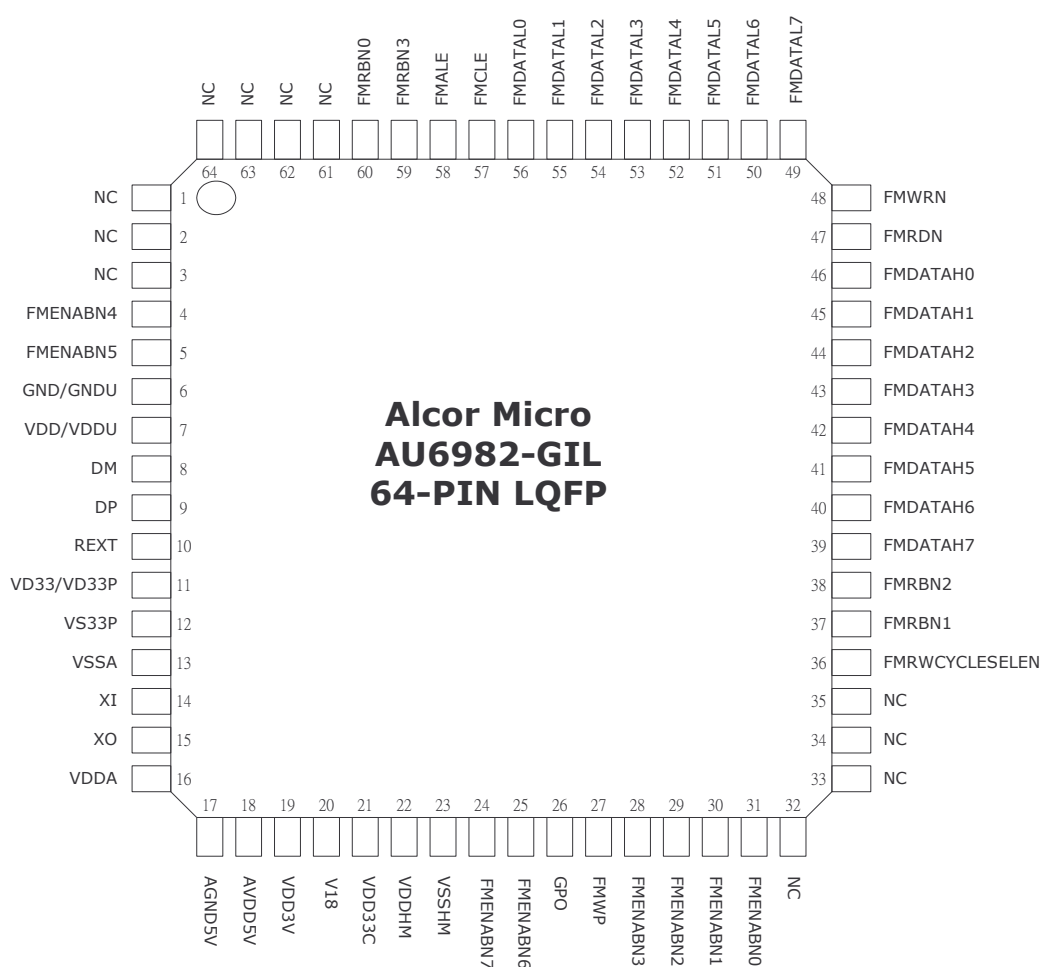
Pin #	Pin Name	I/O	Description
27	FMDATAH7	I/O	Flash Memory DataH[7]
28	FMDATAH6	I/O	Flash Memory DataH[6]
29	FMDATAH5	I/O	Flash Memory DataH[5]
30	FMDATAH4	I/O	Flash Memory DataH[4]
31	FMDATAH3	I/O	Flash Memory DataH[3]
32	FMDATAH2	I/O	Flash Memory DataH[2]
33	FMDATAH1	I/O	Flash Memory DataH[1]
34	FMDATAH0	I/O	Flash Memory DataH[0]
35	FMRDN	I/O	Flash Memory Read Enable; Low Active
36	FMWRN	I/O	Flash Memory Write Enable; Low Active
37	FMDATAL7	I/O	Flash Memory DataL[7]
38	FMDATAL6	I/O	Flash Memory DataL[6]
39	FMDATAL5	I/O	Flash Memory DataL[5]
40	FMDATAL4	I/O	Flash Memory DataL[4]
41	FMDATAL3	I/O	Flash Memory DataL[3]
42	FMDATAL2	I/O	Flash Memory DataL[2]
43	FMDATAL1	I/O	Flash Memory DataL[1]
44	FMDATAL0	I/O	Flash Memory DataL[0]
45	FMCLE	O	Flash Memory Command Latch Enable ;High Active
46	FMALE	O	Flash Memory Address Latch Enable; High Active;
47	FMRBN3	I	Flash Memory(H3) Ready and Busy Signal (1=Ready ; 0=Busy)
48	FMRBN0	I	Flash Memory(H0) Ready and Busy Signal (1=Ready ; 0=Busy)



3.2 64Pin AU6982-GIL

The following figure shows signal names of each pin of the 64-pin package and the table in the page after describes each pin in details.

Figure 3.2 64 Pin Assignment Diagram



**Table 3.2 64 Pin Descriptions**

Pin #	Pin Name	I/O	Description
1	NC		
2	NC		
3	NC		
4	FMENABN4	I/O	Flash Memory #4 Enable; Low Active
5	FMENABN5	I/O	Flash Memory #5 Enable; Low Active
6	GND/GNDU	GND	Ground
7	VDD/GDDU	I	1.8V Power Source for Core / 1.8V Power Source for UTMI
8	DM	I/O	USB DM
9	DP	I/O	USB DP
10	REXT	I	External 330 Resister to Ground
11	VD33/VD33P	I	3.3V Power Source for UTMI
12	VS33P	GND	Ground
13	VSSA	GND	Ground
14	XI	I	12 MHz crystal input.
15	XO	O	12 MHz crystal output.
16	VDDA	I	1.8V Power Source for PLL
17	AGND5V	GND	Ground
18	AVDD5V	I	5V Power Source
19	VDD3V	O	3.3 V Power Out
20	V18	O	1.8V Power Out for Core
21	VDD33C	O	3.3V Power Out for Flash Memory
22	VDDHM	I	3.3V Power Source for IO pad
23	VSSHM	GND	Ground
24	FMENABN7	I/O	Flash Memory #7 Enable; Low Active
25	FMENABN6	I/O	Flash Memory #6 Enable; Low Active
26	GPO	O	General Purpose OutPut
27	FMWP	I	Flash Memory Write Protect; High Active
28	FMENABN3	I/O	Flash Memory #3 Enable; Low Active
29	FMENABN2	I/O	Flash Memory #2 Enable; Low Active
30	FMENABN1	I/O	Flash Memory #1 Enable; Low Active
31	FMENABN0	I/O	Flash Memory #0 Enable; Low Active
32	NC		
33	NC		
34	NC		
35	NC		
36	FMRWCYCLESELEN	I	Flash Memory R/W Cycle Selectionby Jumper; High Active

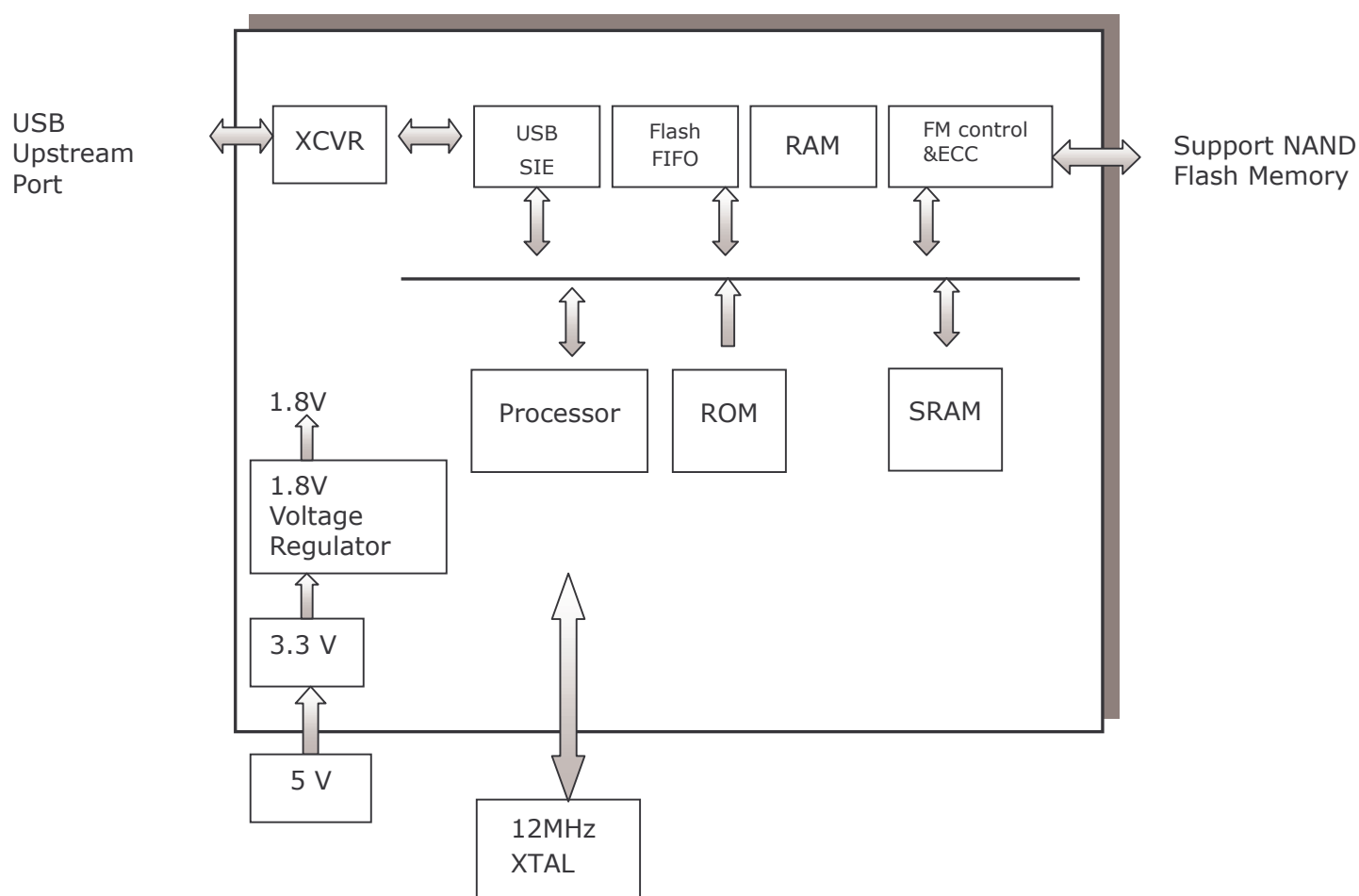


Pin #	Pin Name	I/O	Description
37	FMRBN1	I	Flash Memory(H1) Ready and Busy Signal (1=Ready ; 0=Busy)
38	FMRBN2	I	Flash Memory(H2) Ready and Busy Signal (1=Ready ; 0=Busy)
39	FMDATAH7	I/O	Flash Memory DataH[7]
40	FMDATAH6	I/O	Flash Memory DataH[6]
41	FMDATAH5	I/O	Flash Memory DataH[5]
42	FMDATAH4	I/O	Flash Memory DataH[4]
43	FMDATAH3	I/O	Flash Memory DataH[3]
44	FMDATAH2	I/O	Flash Memory DataH[2]
45	FMDATAH1	I/O	Flash Memory DataH[1]
46	FMDATAH0	I/O	Flash Memory DataH[0]
47	FMRDN	I/O	Flash Memory Read Enable; Low Active
48	FMWRN	I/O	Flash Memory Write Enable; Low Active
49	FMDATAL7	I/O	Flash Memory DataL[7]
50	FMDATAL6	I/O	Flash Memory DataL[6]
51	FMDATAL5	I/O	Flash Memory DataL[5]
52	FMDATAL4	I/O	Flash Memory DataL[4]
53	FMDATAL3	I/O	Flash Memory DataL[3]
54	FMDATAL2	I/O	Flash Memory DataL[2]
55	FMDATAL1	I/O	Flash Memory DataL[1]
56	FMDATAL0	I/O	Flash Memory DataL[0]
57	FMCLE	O	Flash Memory Command Latch Enable ;High Active
58	FMALE	O	Flash Memory Address Latch Enable; High Active;
59	FMRBN3	I	Flash Memory(H3) Ready and Busy Signal (1=Ready ; 0=Busy)
60	FMRBN0	I	Flash Memory(H0) Ready and Busy Signal (1=Ready ; 0=Busy)
61	NC		
62	NC		
63	NC		
64	NC		

4.0 System Architecture and Reference Design

4.1 AU6982 Block Diagram

Figure 4.1 AU6982 Block Diagram





5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDHM}	Power Supply	-0.3 to $V_{DDHM} + 0.3$	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to $V_{DDHM} + 0.3$	V
T_{STG}	Storage Temperature	-40 to 150	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
A_{VDD5V}	5V Power Supply	4.75	5.0	5.25	V
V_{DDHM}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	°C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		pF
C_{OUT}	Output capacitance	Pad Limit		2.8		pF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		pF



5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDHM}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$ I_{ol} = 2 \sim 16\text{mA}$			0.4	V
V_{oh}	Output high voltage	$ I_{oh} = 2 \sim 16\text{mA}$	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	$K\Omega$
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	$K\Omega$
I_{in}	Input leakage current	$V_{in} = V_{DDHM}$ or 0	-10	± 1	10	μA
I_{oz}	Tri-state output leakage current		-10	± 1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VD33	Analog supply Voltage		3.0	3.3	3.6	V
VDDA	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA
$I_{CC(susp)}$	Suspend supply current	In suspend mode, current with 1.5k Ω pull-up resistor on pin RPU disconnected			120	μA



Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V

VD33=3.0V~3.6V ; VDDA =1.62V~1.98V ; Temp=0℃~70℃

Table 5.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V _{HSDIFF}	High speed differential input sensitivity	V _{I (DP)} -V _{I (DM)} measured at the connection as application circuit	300			mV
V _{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V _{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V _{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V _{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V _{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V _{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V _{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V _{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						



R _{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V _{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V _{DI}	Differential input sensitivity	V _{I (DP)} -V _{I (DM)}	0.2			V
V _{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						
V _{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V _{OL}	Low-level output voltage		0		0.3	V
V _{OH}	High-level output voltage		2.8		3.6	V

VD33=3.0V~3.6V ; VDDA =1.62V~1.98V ; Temp=0℃~70℃

Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						

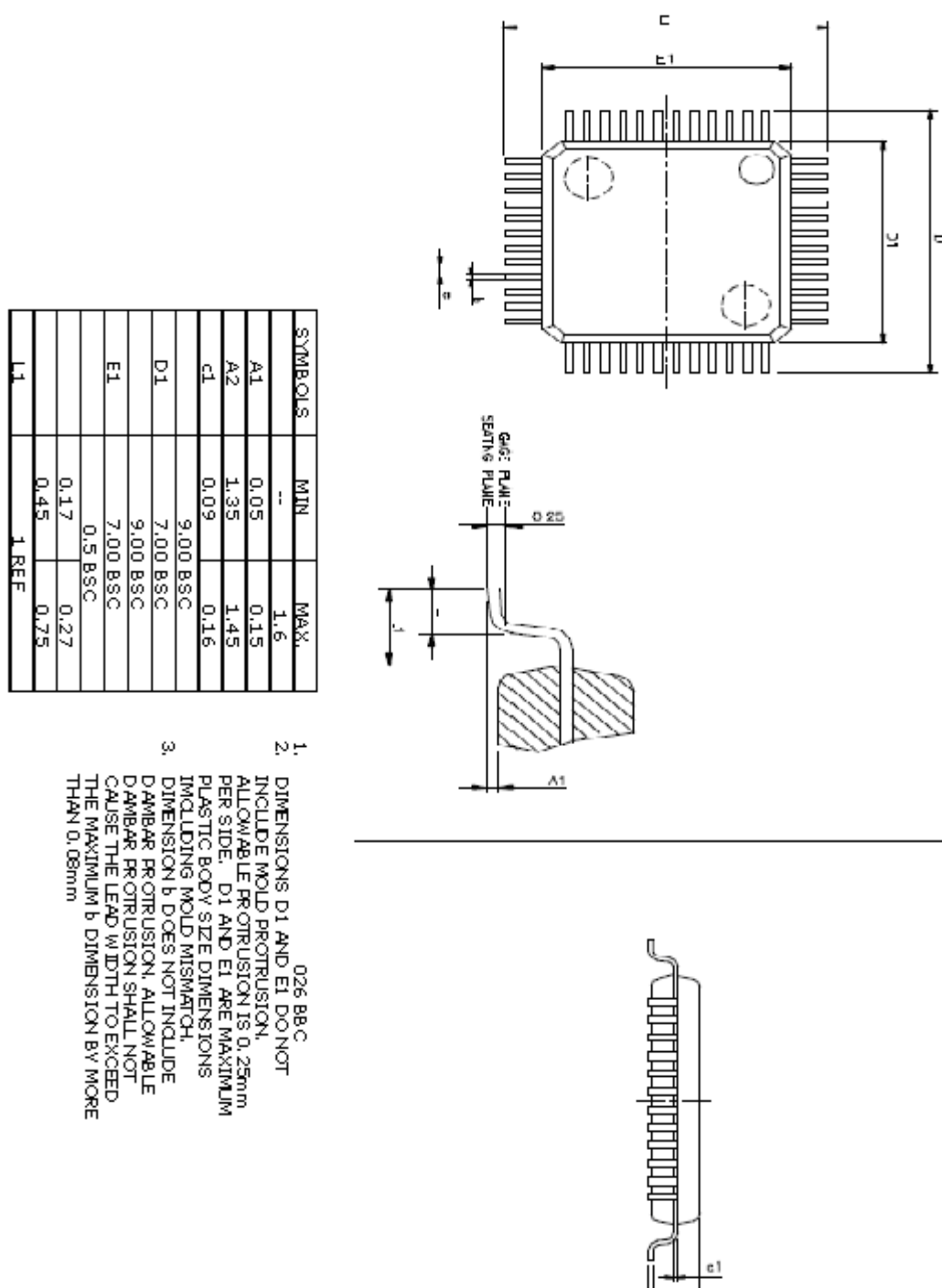


t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

6.1 48Pin AU6982-GHL

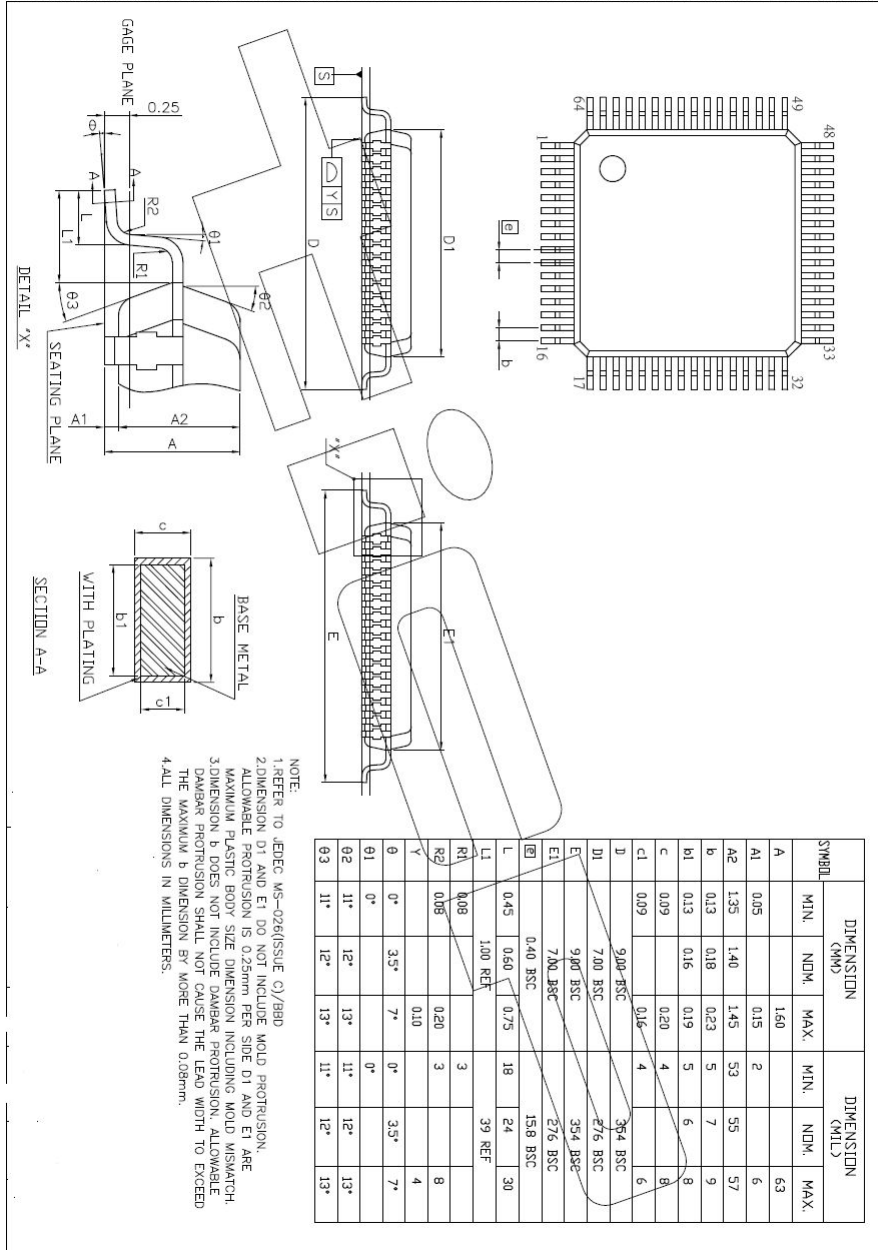
Figure 6.1 48 LQFP Mechanical Information Diagram



6.2 64Pin AU6982-GIL

Figure 6.2 64 LQFP Mechanical Information Diagram

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7.0 Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

DC Electrical	Direct Current Electrical
PLL	Phase Lock Loop, which is a closed-loop frequency control system.
ECC	Error Checking and Correcting
XTAL	Crystal
UFD	USB Flash Disk
iStar	Partition/Password Operation Tool - the smart application program developed by Alcor Micro as a companion handy tool for managing the UFD.



About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader...etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

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